CLAIMS

What is claimed is:

1. A method for providing hint instructions to a processor, comprising the steps of:

generating a hint instruction in response to a set of object code to be executed by the processor;

inserting a break instruction into the object code such that the break instruction causes the processor to obtain and execute the hint instruction.

2. The method of claim 1, wherein the step of inserting a break instruction comprises the step of inserting the break instruction in place of a selected instruction in the object code.

3. The method of claim 2, wherein the step of generating a hint instruction comprises the step of generating a set of hint code which includes the hint instruction and the selected instruction such that the break instruction causes the processor to obtain and execute the hint code.

4. The method of claim 2, wherein the step of generating a hint instruction comprises the step of loading the hint instruction into a hint register such that the break instruction causes the processor to obtain the hint instruction from the hint register and execute the hint instruction.

5. The method of claim 4, wherein the step of loading the hint instruction into a hint register

further includes the step of loading the selected instruction into the hint register such that the break instruction causes the processor to obtain the selected instruction from the hint register and execute the selected instruction.

6. The method of claim 4, wherein the step of loading the hint instruction into a hint register further includes the step of loading an address into the hint register such that the break instruction causes the processor to load the hint register using the address.

7. The method of claim 1, wherein the step of generating a hint instruction comprises the step of determining the hint instruction in response to a micro-architecture of the processor.

8. A computer system, comprising:

object code adapter that determines a hint instruction in response to a set of object code and that inserts a break instruction into the object code;

processor that executes the object code such that the break instruction causes the processor to obtain and executes the hint instruction.

9. The computer system of claim 8, wherein the object code adapter inserts the break instruction in place of a selected instruction in the object code.

10. The computer system of claim 9, wherein the object code adapter generates a set of hint code

which includes the hint instruction and the selected instruction.

11. The computer system of claim 10, wherein the processor branches to the hint code when executing the break instruction.

12. The computer system of claim 9, wherein the processor includes a hint register for holding the hint instruction such that the processor obtains the hint instruction from the hint register and executes the hint instruction in response to the break instruction.

13. The computer system of claim 12, wherein the hint register holds the selected instruction such that the processor obtains the selected instruction from the hint register and executes the selected instruction in response to the break instruction.

14. The computer system of claim 12, wherein the hint register holds an address such that the processor loads the hint register using the address in response to the break instruction.

15. The computer system of claim 8, wherein the object code adapter determines the hint instruction in response to a micro-architecture of the processor.